

WHAT IS CLAIMED IS:

1. A semiconductor device having a copper (Cu) or Cu alloy interconnect comprising:
an opening formed in a dielectric layer;
a tantalum nitride (TaN) layer lining the opening;
a graded tantalum nitride layer on the TaN layer;
a continuous layer of α - tantalum (α -Ta) on the graded tantalum nitride layer; and
Cu or Cu alloy filling the opening, wherein the ratio of the thickness of the combined α -Ta and graded tantalum nitride layers to the thickness of the TaN layer is about 2:1 to about 6:1.
2. The semiconductor device according to claim 1, wherein the ratio is about 2.5:1 to about 3.5:1.
3. The semiconductor device according to claim 1, wherein the TaN layer has a thickness of about 50 Å to about 100 Å.
4. The semiconductor device according to claim 3, wherein the continuous α -Ta layer has a thickness of about 200 Å to about 300 Å.
5. The semiconductor device according to claim 1, wherein:
the opening is a dual damascene opening; and
the interconnect structure comprises a lower Cu or Cu alloy via connected to an upper Cu or Cu alloy line.
6. The semiconductor device according to claim 5, wherein the dielectric material has a dielectric constant less than about 3.9.
7. The semiconductor device according to claim 1, wherein the graded tantalum nitride layer contains α -Ta ranging from about zero proximate the TaN layer to about 100% proximate the continuous α -Ta layer.

8. The semiconductor device according to claim 1, wherein:
the TaN layer contains about 30 to about 65 at.% nitrogen (N₂); and
the N₂ concentration of the graded tantalum nitride layer ranges from about 30 to about 65 at.% proximate the TaN layer to about 0 proximate the continuous α -Ta layer.

9. The semiconductor device according to claim 1, wherein the TaN, graded tantalum nitride and continuous α -Ta layers have a combined thickness of about 250 Å to about 500 Å.

10. The semiconductor device according to claim 2, wherein the opening is a dual damascene opening and the interconnect structure comprises a lower Cu or Cu alloy via in electrical contact with a lower metal feature and connected to an upper Cu or Cu alloy line.

11. The semiconductor device according to claim 10, wherein the interlayer dielectric comprises a dielectric material having a dielectric constant less than about 3.9.